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A Simplified, General-Purpose Deep-Space Ranging Correlator Design

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This article describes a much-simplified, yet more general-purpose multi-channel deep-space ranging system correlator design than has been used in past JPL spacecraft ranging systems. The method applies to detection of both single-component and multiple-component ranging codes, in either sequential (μ) or composite (τ) transmitted forms, and using either pseudonoise or square-wave components. Using this design, the Phobos Probe ranging system correlator computational complexity was reduced by over three orders of magnitude in multiply-and-add circuits and 45,000 bits of accumulator storage.

I. Introduction and Background

JPL Spacecraft ranging systems transmit, from the ground to the spacecraft, a periodic code $x(t)$ modulated on the uplink carrier. This signal received by the on-board transponder, is demodulated and retransmitted via the downlink to the ground station. The received version of the transmitted code at the ranging demodulator assembly interface appears attenuated by a factor α, delayed by the round-trip light-time τ(continuously changing due to the earth and spacecraft relative velocity), and immersed in noise, $n(t)$. Symbolically,

$$y(t) = \alpha x(t-\tau) + n(t) \tag{1}$$

Present DSN ranging systems [1] use the two-way detected Doppler signal from the receiver to program the clock oscillators of the receiver codes, generating replicas of the transmitted-code component(s) to maintain a constant value of τ between the received signal, $y(t)$, and the local receiver codes.

The optimum [2] estimate in the maximum-likelihood sense, $\hat{\tau}$, for the time delay τ over a given observation interval $[0, T]$, set by ranging accuracy requirements and the incoming signal-to-noise ratio,[1] is that value maximizing the cross-correlation integral

$$I_{\hat{\tau}} = \int_0^T y(t)c(t-\hat{\tau})\,dt \tag{2}$$

[1] Typically minutes to hours in duration.

where $c(t)$ denotes a particular code component of the transmitted signal, $x(t)$. Computation of $l_{\hat{\tau}}$ thus requires a ground receiver channel equivalent to the form shown in Fig. 1.

To determine $\hat{\tau}$, a set $\{\hat{\tau}_i : i = 0, \ldots, N-1\}$ of candidate code-delay values is chosen and used to measure corresponding "correlation-lag" values $\{l_{\hat{\tau}_i} : i = 0, \ldots, N-1\}$, which are then inserted into a maximum-likelihood formula for determining $\hat{\tau}$.

The ranging codes are binary ±1-valued signals having a symbol-interval time we denote by t_0. As explained in a companion article [3], the transmitted waveform is either a Boolean function of several pseudonoise [4] binary sequences running in parallel (the so-called composite-code approach [1]) or a sequence of binary square waves of increasingly short periods (the sequential-code approach). For historical reasons, these were dubbed "τ" and "μ" methods, respectively.

The first planetary ranging system [5] utilized a combined-component-code uplink scheme that required 77 receiver correlations, but only had 2 channels. It was used on Mariner missions from 1969 through 1973, and was then replaced by sequential-component-code machines [1] because of their superior ranging acquisition time advantage of some 12 dB with only 2 correlation channels, at some extra complexity in receiver code switching and housekeeping logic, and at a modest 1.75–2.75 dB loss factor from the optimum matched filter performance.

The acquisition-time advantage of the μ system came from the feasibility of building ranging correlator channels for each of the needed τ_i of the μ code (*viz.*, 2). The τ scheme would have required 77 such channels, a need without cost justification in that era. The merits of the various transmitter codes and receiver detection schemes are adequately treated elsewhere [1], [4], [6], and are not further discussed here.

For determining the phase of incoming symbol transitions, a "clock" component, or period-2 code, is transmitted in both τ and μ systems. The receiver correlation delays are chosen to be $\hat{\tau}_0 = 0$ and $\hat{\tau}_1 = t_0/2$, with $N = 2$.

For a pseudonoise-sequence code [6] of period p bits, the candidate delay values are $\hat{\tau}_i = it_0/k$ for $i = 0, \ldots, N-1$, with $N = kp$. The integer k may be 1 or 2 or more, depending on the transmitter encoding and the method used to determine the received symbol-transition phase, i.e., the code clock delay.

In any case, in order to compute the N values required, either N correlator channels are required to calculate the $l_{\hat{\tau}_i}$ in parallel, or some lesser number may be used serially, but thereby increasing the acquisition time (equivalently, lowering the effective signal-to-noise ratio).

II. Conventional Ranging Detectors

Conventional DSN ranging correlators are made up of analog and digital hardware and software that mirror the direct calculation of the integral above. Separation into analog and digital portions derives from the following transformation of the correlation integral:

$$l_{\hat{\tau}_i} = \sum_{j=0}^{Mpk-1} c_{j-i} \int_0^{t_0/k} y\left(\frac{t + jt_0}{k}\right) dt \qquad (3)$$

where the integration time T is assumed to be a multiple of the period, the code delay $\hat{\tau}_i$ is assumed to be a multiple of the fractional symbol interval, and the coefficients c_j represent the ±1 code symbol values,

$$\begin{aligned} T &= Mpt_0 = Mpkt_0/k \\ \hat{\tau}_i &= it_0/k \\ c_j &= c_m \text{ when } \lfloor j/k \rfloor \equiv \lfloor m/k \rfloor \ (\mathrm{mod}\ p) \\ c_{kj} &= c(jt_0) \text{ for } j = 0, \ldots, p-1 \end{aligned}$$

The integral thus represents the sum of integrations of the incoming signal over fractional code symbol intervals, multiplied by the appropriate code symbol values over those intervals. One such sum is required for each channel delay $\hat{\tau}_i$, and all multiply's and add's occur in parallel with each other.

The conventional design of a multi-channel range detector is depicted in Fig. 2. Both the old τ and later μ machines used this design, with 2 physical correlator channels. Integration over fractional symbol times is performed by analog hardware, and only one such integrator is needed. The integration value is sampled and converted to a digital number, multiplied by the N delayed code ±1 stream values, and added to the contents of N accumulators, once each fractional symbol time.

Since k consecutive c_{j-i} values are equal, these sample values may be preaccumulated before multiplications, if desired. This, in fact, is done in the current DSN Spacecraft Ranging System. However, the high-speed logic required for processing the pre-accumulation and subsequent parallel multiply-and-add operations contributes significantly to the ranging assembly cost.

The advent of fast, custom-made, Very Large Scale Integration (VLSI) components has made it possible, albeit still moderately costly, to build many more correlator channels using the same form of digital design as shown in Fig. 2, so that all the needed correlation-delay values can be accumulated digitally in parallel [3].

As a case in point, the ranging uplink design for the Phobos Probe mission uses a pseudonoise code of period 2047, transmitted at about 1.2×10^6 symbols per second. A ranging correlator design using the conventional approach, using only $k = 2$ samples per code symbol, would require nearly 5×10^9 multiply-and-add operations per second. In fact, a preliminary design using the conventional approach was made; it required a massively parallel pipelined architecture utilizing the fastest available memory circuits, and still had to resort to 1-bit quantization of the input signal in order to simplify the multiplier design, with a corresponding 2 dB loss in signal-to-noise performance.

The economics and technology requirements of this conventional approach thus place limits on the code period and performance that can reasonably be expected.

III. The Simplified Digital Correlator

In this section, we note that the correlation integral may be further transformed to reverse the order of digital accumulation and multiplication in calculating the various needed measurements. The advantage of this reversal, as we shall see, is that it reduces the amount of high-speed digital logic and custom-VLSI chips needed, removes almost all of the ranging code dependency from the ranging demodulator hardware, and makes possible the design of a general-purpose ranging demodulator capable of accumulating thousands of correlation-lag values.

By making use of the periodicity of the receiver code, the correlation integral may be further transformed into the equation

$$I_{\hat{\tau}_i} = \sum_{j=0}^{pk-1} c_{j-i} \sum_{m=0}^{M-1} \int_0^{t_0/k} y\left(t + \frac{(j+mpk)t_0}{k}\right) dt \tag{4}$$

or merely

$$I_{\hat{\tau}_i} = \sum_{j=0}^{pk-1} c_{j-i} A_j \tag{5}$$

where A_j represents the accumulation of integrate-and-dump values,

$$A_j = \sum_{m=0}^{M-1} \int_0^{t_0/k} y\left(t + \frac{(j+mpk)t_0}{k}\right) dt \tag{6}$$

The revised correlator depicted in Fig. 3 utilizes pk accumulators for the $\{A_j, j = 0, \ldots, pk - 1\}$ values. Note that each integrator sample output is added only into one of the accumulator channels, switched by the accumulator index j, each t_0/k seconds. Because of this simplification, only one adder is required for all the accumulators corresponding to this receiver code, as shown in Fig. 4. This functionally saves $pk - 1$ multiply-and-add logic circuits (4093 of them for the Phobos Probe mission).

For each integrator sample, the corresponding accumulator is fetched, added to the sample, and restored into memory. Each accumulator is only accessed once each pt_0 time interval. Using this technique, the redesigned Phobos Probe ranging correlator requires only 2.4×10^6 additions per second. As a result, conventional Random Access Memory circuitry can be used to hold the values.

Moreover, the accumulators are in jeopardy of overflow only $1/p$ as much as in the conventional design. Consequently, each accumulator can be shorter by $\log_2(p)$ bits than those of the conventional design. This represents an additional logic savings of $pk \log_2(p)$ bits, or about 45,000 bits (5600 bytes) in the Phobos Probe ranging correlator storage.

The address generator is merely a counter clocked at the code fractional symbol rate and reset at the beginning of each period of the receiver code. This is the only code-dependent signal entering the digital portion of the design. Except for the number of lag-value accumulators, the digital portion of the correlator assembly is completely independent of the receiver code components. No receiver coder hardware is necessary. Conventional deep-space ranging correlators required hardware code generators for each of the different receiver code components.

Code multiplications are not made until after the complete accumulation of A_j values has been read into the computer of the ranging assembly. Then the same A_i set serves to calculate all of the $I_{\hat{\tau}_i}$ for $i = 0, \ldots, N - 1$. The vector **I** containing the $I_{\hat{\tau}_i}$ is related to the vector **A** of accumulator values A_i by the equation

$$\mathbf{I} = \mathbf{CA} \tag{7}$$

where **C** is the $N \times kp$ matrix of binary code values, $c_{i,j} = c_{j-i}$. Since the receiver codes are stored solely in the computer memory as **C**, since the vector **I** is computed separately from the accumulation process, and since this computation only needs to take place infrequently, there is a greater degree of flexibility and generality in the simpler design than existed in the previous ranging assemblies.

IV. Conclusion

This article has presented a design simplification for the digital hardware design of a deep-space binary-code ranging system. The simplification is significant in that it

(1) Makes use of easily obtainable RAM storage, one memory location for each correlation lag to be accumulated, accessed serially, rather than special VLSI devices or high-speed-logic circuits accessed in parallel;

(2) Reduces the high-speed digital logic requirements to a single sample accumulator and adder, regardless of the number of correlation lags computed, representing a savings of $pk - 1$ multiply-and-add circuits;

(3) Reduces the number of bits required by each accumulator by $\log_2(p)$ bits each, for a savings of $pk \log_2(p)$ bits for the entire correlator;

(4) Makes the analog and digital portions of the system independent of both the transmitter and receiver codes, except for timing signals;

(5) Removes the need for receiver coders (simple period counters will do); and

(6) Stores the receiver code component(s) as a vector in the ranging computer, where the accumulated correlation-lag values are computed by a single simple matrix multiplication, infrequently calculated.

Using this approach, the new Phobos Probe mission ranging system design uses no special components, is smaller, is easier to design and maintain, and does not need to 1-bit quantize the input signal. The details and particulars of the correlator design will be the subject of a subsequent article.

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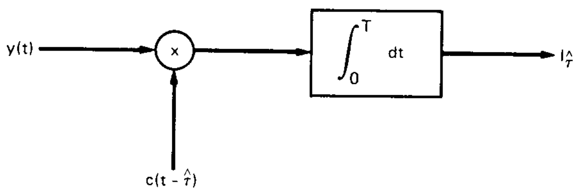

Fig. 1. Ranging correlator channel functional design

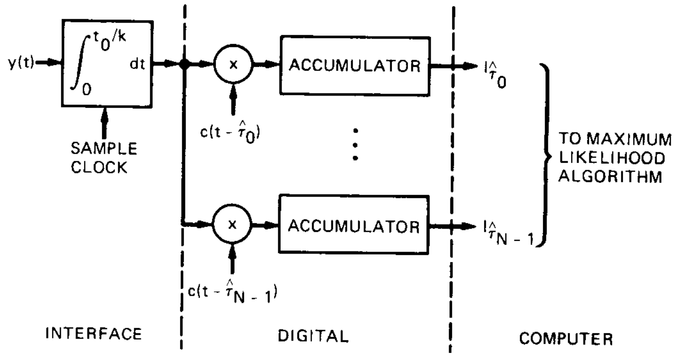

Fig. 2. Conventional multi-channel ranging correlator design

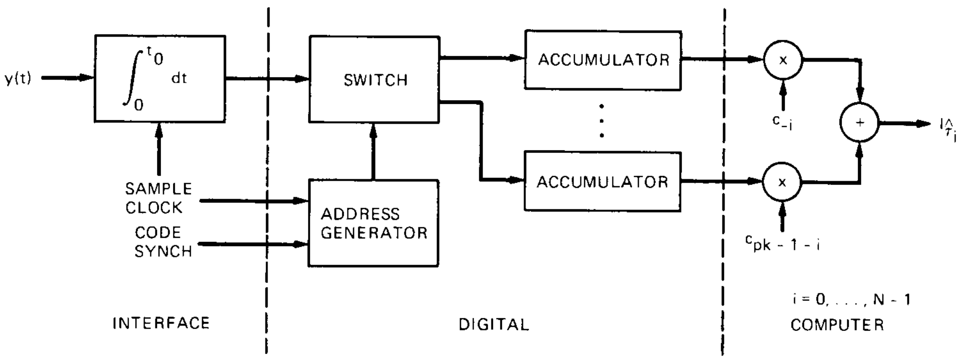

Fig. 3. Revised multi-channel ranging correlator design

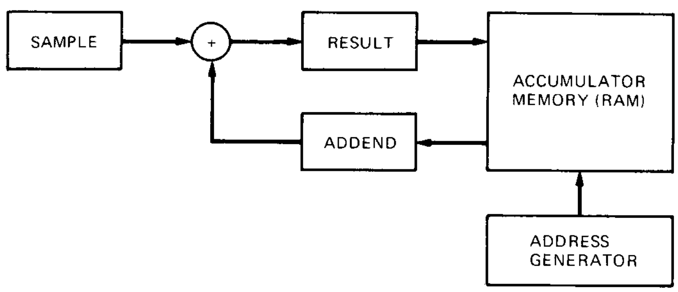

Fig. 4. Ranging correlator digital processor